

Table 1-2 lists Cyclone IV GX device resources.

**Table 1-2. Resources for the Cyclone IV GX Device Family**

Resources	EP4CGX15	EP4CGX22	EP4CGX30 <sup>(1)</sup>	EP4CGX30 <sup>(2)</sup>	EP4CGX50 <sup>(3)</sup>	EP4CGX75 <sup>(3)</sup>	EP4CGX110 <sup>(3)</sup>	EP4CGX150 <sup>(3)</sup>
Logic elements (LEs)	14,400	21,280	29,440	29,440	49,888	73,920	109,424	149,760
Embedded memory (Kbits)	540	756	1,080	1,080	2,502	4,158	5,490	6,480
Embedded 18 × 18 multipliers	0	40	80	80	140	198	280	360
General purpose PLLs	1	2	2	4 <sup>(4)</sup>	4 <sup>(4)</sup>	4 <sup>(4)</sup>	4 <sup>(4)</sup>	4 <sup>(4)</sup>
Multipurpose PLLs	2 <sup>(5)</sup>	2 <sup>(5)</sup>	2 <sup>(5)</sup>	2 <sup>(5)</sup>	4 <sup>(5)</sup>	4 <sup>(5)</sup>	4 <sup>(5)</sup>	4 <sup>(5)</sup>
Global clock networks	20	20	20	30	30	30	30	30
High-speed transceivers <sup>(6)</sup>	2	4	4	4	8	8	8	8
Transceiver maximum data rate (Gbps)	2.5	2.5	2.5	3.125	3.125	3.125	3.125	3.125
PCIe (PIPE) hard IP blocks	1	1	1	1	1	1	1	1
User I/O banks	9 <sup>(7)</sup>	9 <sup>(7)</sup>	9 <sup>(7)</sup>	11 <sup>(8)</sup>	11 <sup>(8)</sup>	11 <sup>(8)</sup>	11 <sup>(8)</sup>	11 <sup>(8)</sup>
Maximum user I/O <sup>(9)</sup>	72	150	150	290	310	310	475	475

**Notes to Table 1-2:**

- (1) Applicable for the F169 and F324 packages.
- (2) Applicable for the F484 package.
- (3) Only two multipurpose PLLs for F484 package.
- (4) Two of the general purpose PLLs are able to support transceiver clocking. For more information, refer to the [Clock Networks and PLLs in Cyclone IV Devices](#) chapter.
- (5) You can use the multipurpose PLLs for general purpose clocking when they are not used to clock the transceivers. For more information, refer to the [Clock Networks and PLLs in Cyclone IV Devices](#) chapter.
- (6) If PCIe ×1, you can use the remaining transceivers in a quad for other protocols at the same or different data rates.
- (7) Including one configuration I/O bank and two dedicated clock input I/O banks for HSSI reference clock input.
- (8) Including one configuration I/O bank and four dedicated clock input I/O banks for HSSI reference clock input.
- (9) The user I/Os count from pin-out files includes all general purpose I/O, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

## New FPGA:

### Device Resources

Table 1–1 lists Cyclone IV E device resources.

**Table 1–1. Resources for the Cyclone IV E Device Family**

Resources	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Logic elements (LEs)	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
Embedded memory (Kbits)	270	414	504	594	594	1,134	2,340	2,745	3,888
Embedded 18 × 18 multipliers	15	23	56	66	66	116	154	200	266
General-purpose PLLs	2	2	4	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20	20
User I/O Banks	8	8	8	8	8	8	8	8	8
Maximum user I/O <sup>(1)</sup>	179	179	343	153	532	532	374	426	528

**Note to Table 1–1:**

- (1) The user I/Os count from pin-out files includes all general purpose I/O, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

## Reference and Ordering Information

Figure 1-2 shows the ordering codes for Cyclone IV GX devices.

Figure 1-2. Packaging Ordering Information for the Cyclone IV GX Device

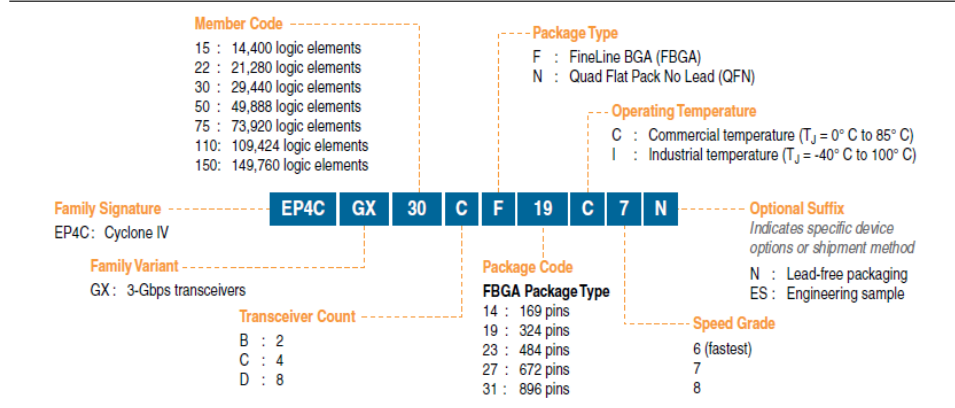


Figure 1-3 shows the ordering codes for Cyclone IV E devices.

Figure 1-3. Packaging Ordering Information for the Cyclone IV E Device

