

The ANAN-100/D HF & 6M Software Defined Radios

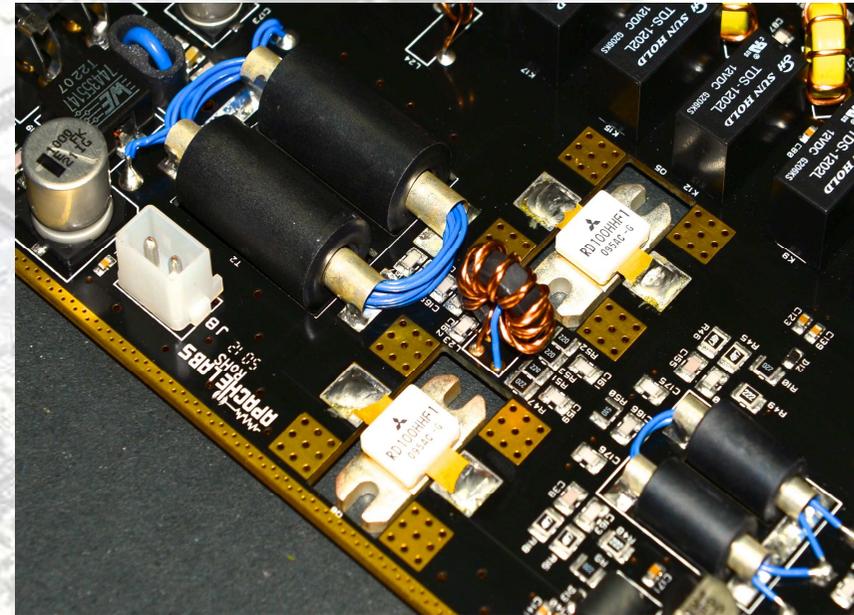
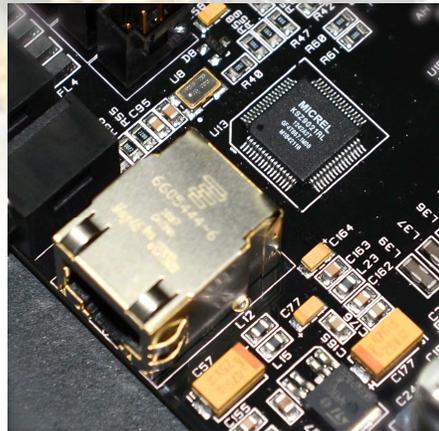
The ANAN-100 & ANAN-100D radios define a new level of performance in Amateur Radio transceivers, based on the very popular OpenHPSDR Hermes and Angelia (ANAN-100D) represent the state-of-the-art in the amateur HF radio space,



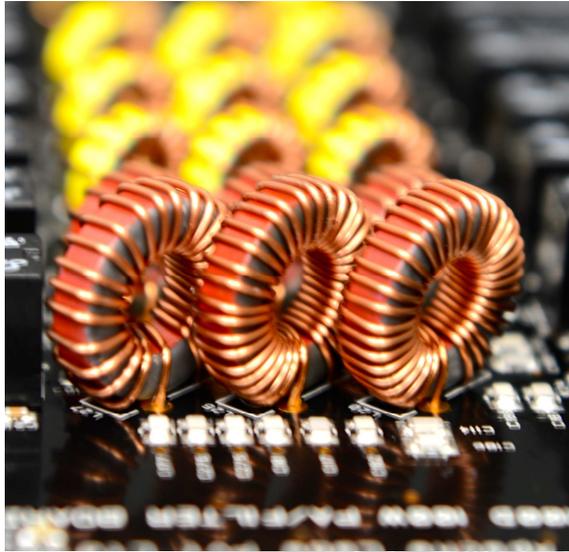
The ANAN-100D is the first HF transceiver with a true phase coherent dual front end comprising of two 16 bit 130MSPS ADCs and a large Cyclone IV FPGA which allows for a huge amount of headroom and DSP processing power, the current

firmware incorporating 14 receivers and diversity reception uses around 30% of the FPGA resources!

Both transceivers use a Gigabit Ethernet interface to connect to the outside world, this means no drivers, huge bandwidth, better noise isolation from the PC and networked radios with remote access and much more. The PC to SDR cable can be longer or you can go wireless and connect the radio to your Wi-Fi and use the radio from anywhere in your home or office.



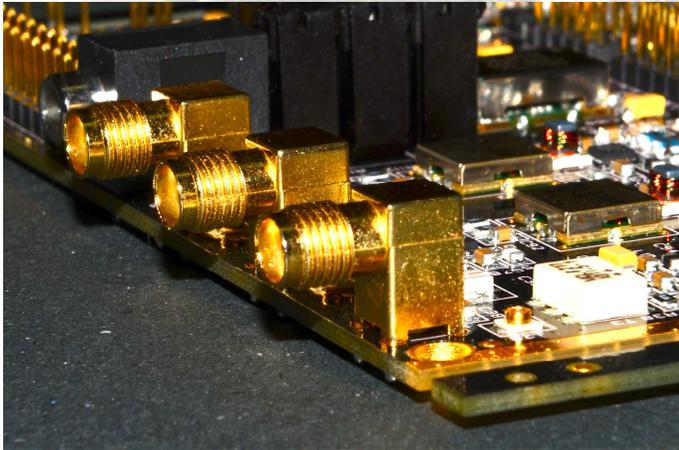
Both radios use rugged Mosfets for the 100W Power Amplifier, our PA design uses custom input/output transformation designed for an almost flat gain response from 160M through 6M, unlike other radios the IMD is -31dB below PEP even on 6M, the entire housing is a single piece aluminium extrusion and heat sink for the PA, resulting in very effective cooling and minimal fan noise.



Unlike conventional radios where front end filtering is at the cost of degraded receiver IMD due to the small BPF inductors and less than optimum filter shape factor (low Q circuits) the ANAN-100/D uses a combination of LPF/HPF banks with oversized toroids to achieve excellent BPF shape factor without effecting the IMD

of the receiver.

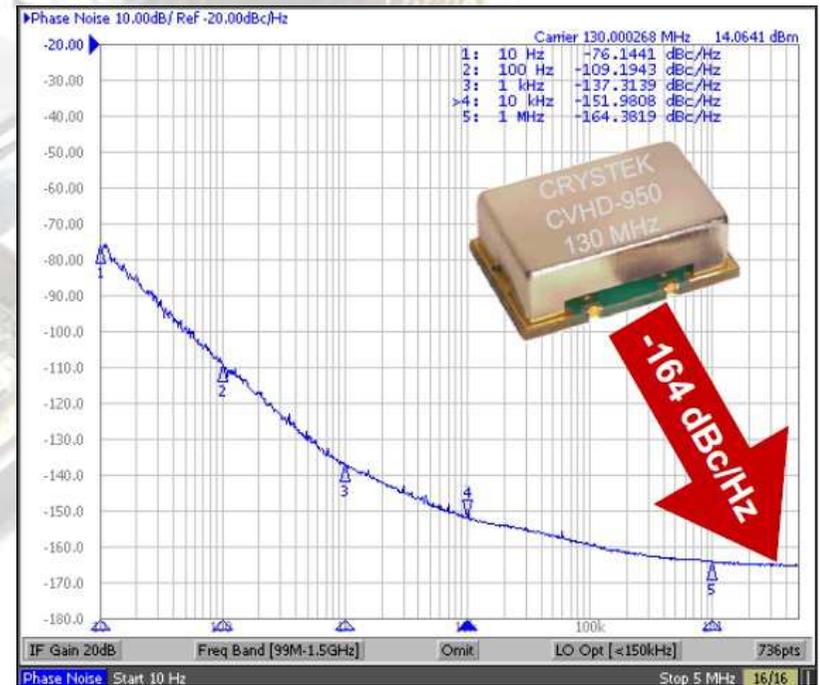
The ANAN radios use gold plated connectors for all RF connections resulting in improved performance and increased dependability.

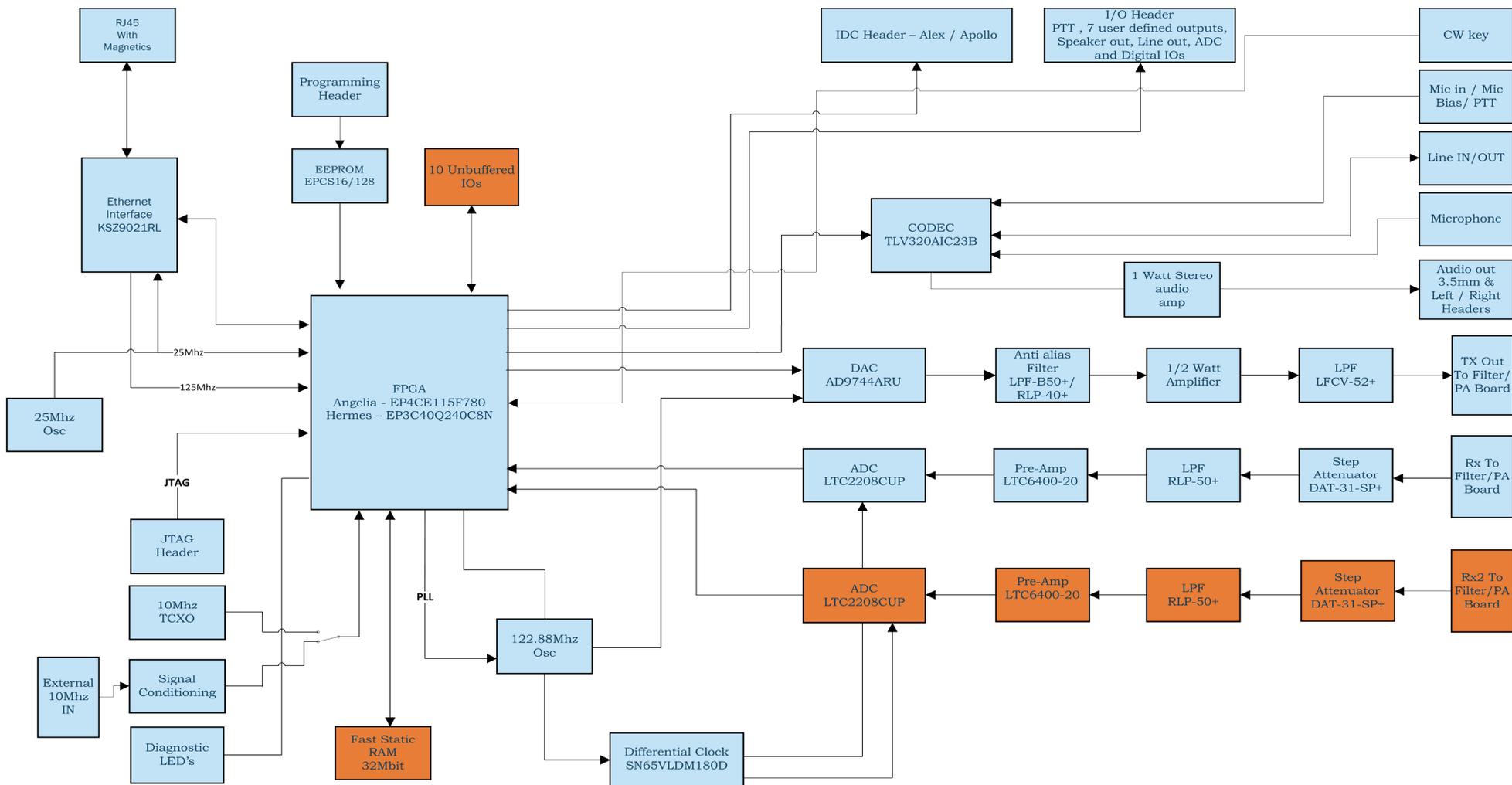


The large FPGA inside the ANAN-100D opens up the possibility of

providing a soft core processor such as the Altera Nios (r) II if desired.

With a very high dynamic range of over 120dB and an IP3 of +50dB (preamp off) the limiting factor could be the LO phase noise, keeping this in mind the designers have used an extremely low noise TCXO, when phase locked with the 10Mhz TCXO the phase noise at 200Hz is < -130dB/HZ

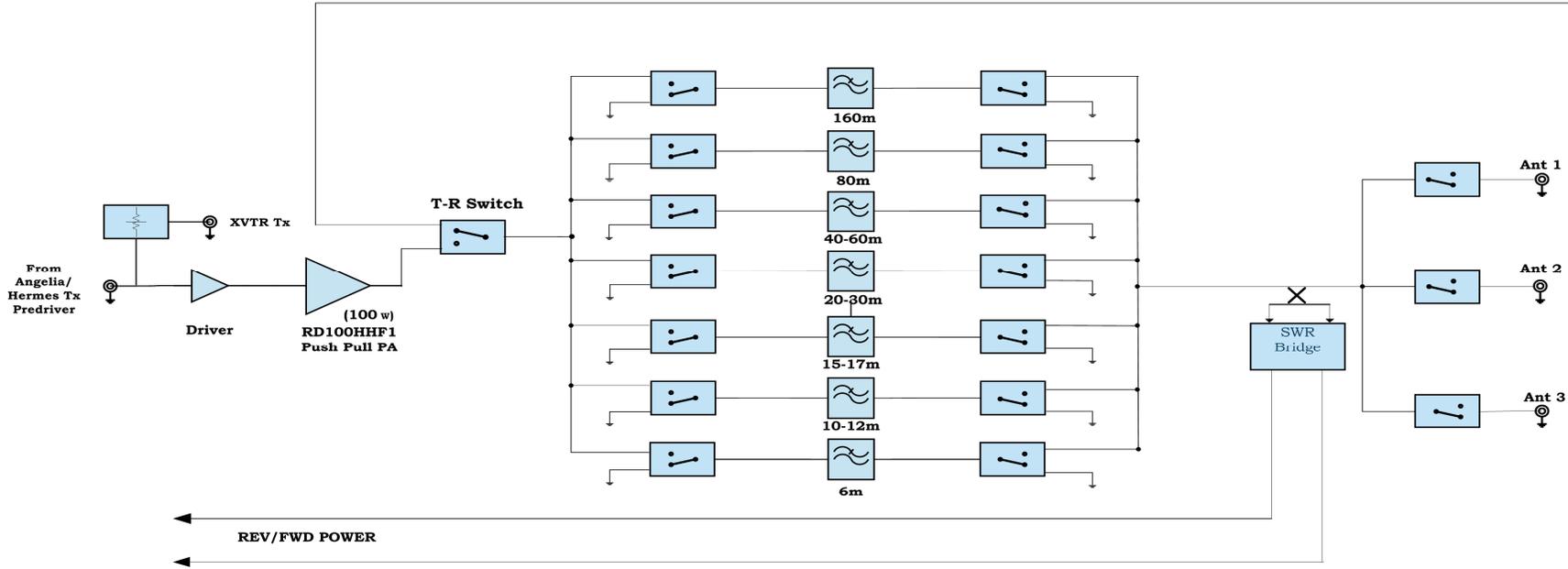
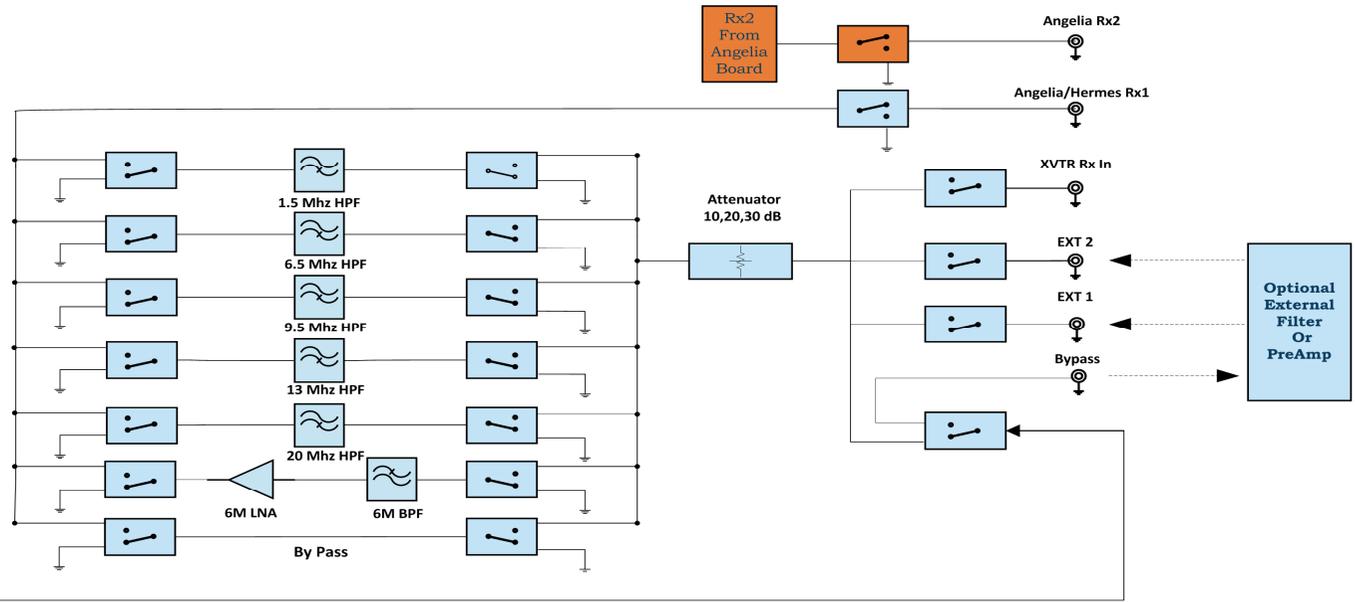
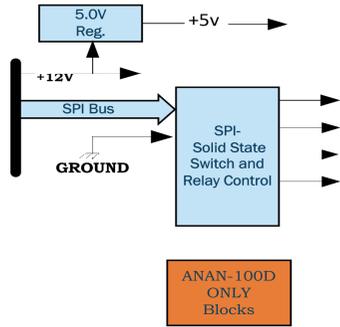


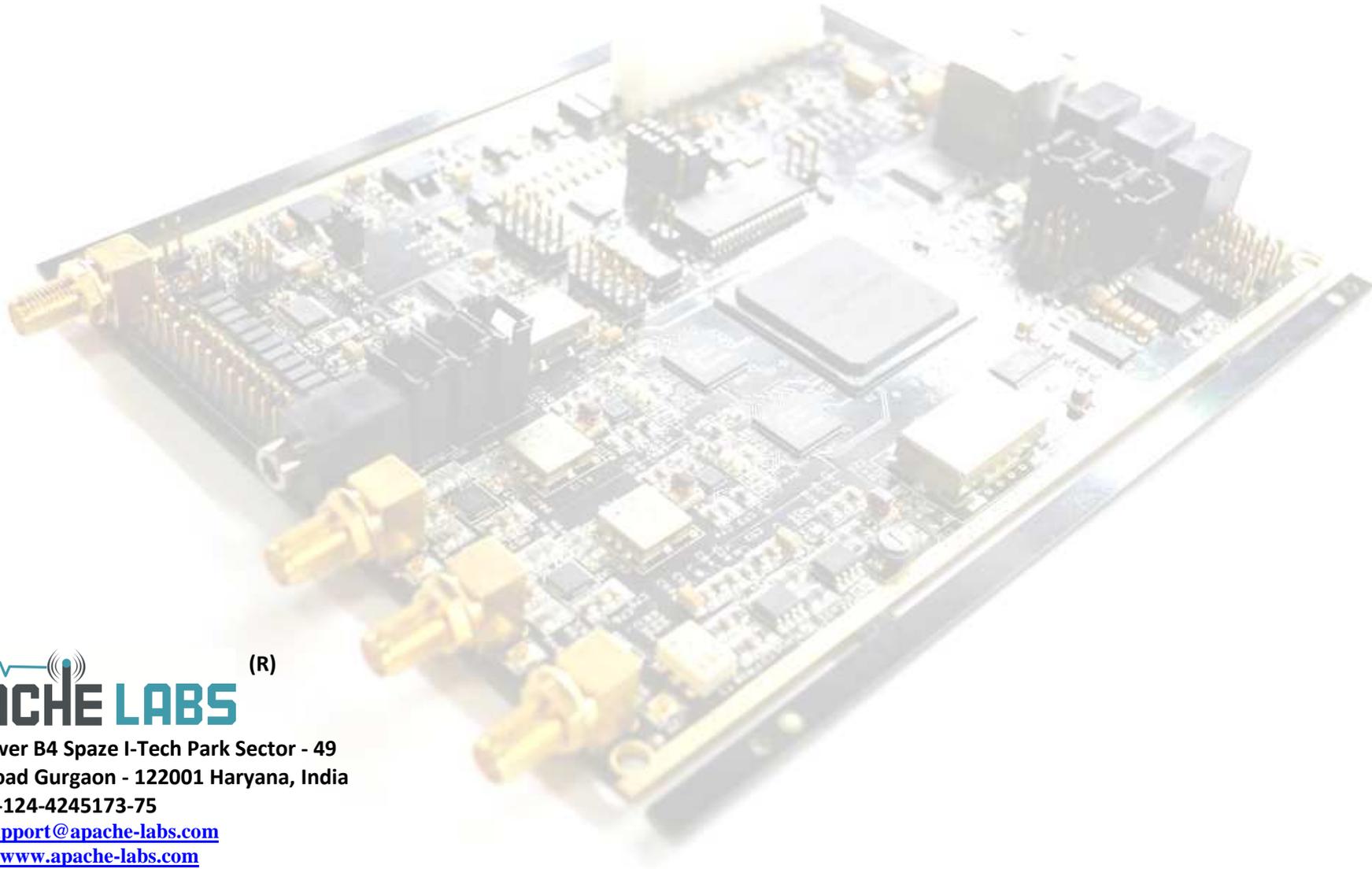


- Regulator 1.2V
- Regulator 2.5V
- Signal Conditioning
- Separate 2A fuses
- Power switch
- ATX Power supply header
- ANAN-100D ONLY Blocks



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100W PA & Filter Board





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